CLAIMS

What is claimed is:

1. An integrated circuit (IC) including at least one combinational logic path, said at least one combinational logic path comprising a plurality of logic blocks, at least one of said logic blocks being a first type cell and at least one other of said logic blocks being a second type cell, a fabrication parameter having a first effect on said first type cell and a second effect on said second type cell.

2. An IC as in claim 1 wherein said second effect is opposite said first effect.

3. An IC as in claim 2 wherein said logic blocks are CMOS logic circuits, each comprising one or more field effect transistors (FETs).

4. An IC as in claim 3 wherein at least one said first type cell includes at least one FET tied off.

5. An IC as in claim 3 wherein said first cell type is a dense cell type, FET gates being on contact pitch within each said dense cell.

6. An IC as in claim 5 wherein said second cell type is an isolated cell type, FET gates being on a pitch greater than said contact pitch within each said isolated cell.

7. An IC as in claim 4 wherein said fabrication parameter is focus variation for an FET gate layer.

8. An IC as in claim 7 wherein said first effect is an increase in block delay from said FET gate layer being printed out of focus.

9. An IC as in claim 8 wherein said first cell type is a dense cell type, FET gates being on contact pitch within each said dense cell and said second cell type is an isolated cell type, FET gates being on a pitch greater than said contact pitch within each said isolated cell, whereby cumulative increase in block delay for each said dense cell in said at least one combinational logic path is offset by cumulative decrease in block delay for each said isolated cell in said at least one combinational logic path.

10. An IC as in claim 8 further comprising at least one second combinational logic path, said at least one second combinational logic path consisting of a plurality dense logic cells, power in said at least one second logic path being reduced from said FET gate layer being printed out of focus.

11. An IC as in claim 1 wherein IC is a standard cell IC.

12. An integrated circuit (IC) including at least one combinational logic path, said at least one combinational logic path comprising a plurality of logic blocks, at least one layer in said at least one logic path having areas of contacted pitch shapes and areas of shapes spaced wider than said contacted pitch.

13. An IC as in claim 12 wherein said logic blocks are CMOS logic circuits, each comprising one or more field effect transistors (FETs).

14. An IC as in claim 13 wherein logic blocks include at least one dense cell and at least one isolated cell, said contacted pitch shapes being in dense cells, delay changes in said dense cells from said at least one layer printing out-of-focus being offset by delay changes in isolated cells.

15. An IC as in claim 14 wherein said delay changes in said dense cells are increases in dense cell delays.

16. An IC as in claim 14 wherein at least one said dense cell is the same logic circuit as at least one said isolated cell.

17. An IC as in claim 14 wherein said at least one layer is a FET gate layer.

18. An IC as in claim 17 wherein at least one said dense cell includes at least one shape not included in a logic circuit, FET gates in said dense cell being on said contacted pitch with said at least one shape and, being on a pitch wider than said contacted pitch without said at least one shape.

19. An IC as in claim 18 wherein said at least one shape in at least one said dense cell is the gate of an FET tied off.

20. An IC as in claim 14 further comprising at least one second combinational logic path, said at least one second combinational logic path consisting of a plurality dense logic cells, power in said at least one second logic path being reduced from said FET gate layer being printed out of focus.

21. An IC as in claim 12 wherein IC is a standard cell IC.

22. A standard cell CMOS integrated circuit (IC) chip, at least one combinational logic path comprising a plurality of standard cell logic blocks, said plurality of logic blocks including at least one dense cell and at least one isolated cell, gate layer shapes in said dense cell being on a contacted pitch and gate layer shapes in said isolated cell being on a pitch wider than said contacted pitch, whereby delay changes in said dense cells from said gate layer shapes being printed out-of-focus being offset by delay changes in isolated cells.

23. A standard cell CMOS IC chip as in claim 22 wherein said logic blocks are logic circuits, each comprising one or more field effect transistors (FETs).

24. An standard cell CMOS IC chip as in claim 23 wherein sàid delay changes in said dense cells are increases in dense cell delays.

25. An standard cell CMOS IC chip as in claim 24 wherein at least one said dense cell is the same logic circuit as at least one said isolated cell.

26. An standard cell CMOS IC chip as in claim 24 wherein at least one said dense cell includes at least one shape not included in a logic circuit, FET gates in said dense cell being on said contacted pitch with said at least one shape and, being on a pitch wider than said contacted pitch without said at least one shape.

27. An standard cell CMOS IC chip as in claim 26 wherein said at least one shape in at least one said dense cell is the gate of an FET tied gate to source.

28. An standard cell CMOS IC chip as in claim 23 further comprising at least one second combinational logic path, said at least one second combinational logic path consisting of a plurality dense logic cells, power in said at least one second logic path being reduced from said FET gate layer being printed out of focus.